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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,785	09/29/2003	Atsushi Date	03500.017602.	7534

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EXAMINER	
FIEGLE, RYAN PAUL	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,785	DATE, ATSUSHI	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 7-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/25/06 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3 and 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Booker et al. (US Patent 6,347,294).

4. As per claim 1:

A processor system on a single semiconductor substrate, wherein the processor system is provided with a built-in processor (column 3, lines 33-38), a memory controller (column 4, lines 9-15; Figure 2, item 126), an external bus interface that can connect an

external processor from outside of a single semiconductor substrate (column 3, lines 39-52), a processor bus which is connected with the built-in processor and the external bus interface (column 4, lines 32-36; Figure 2/3, item 152), and a connection unit that mutually connects, the memory controller and the processor bus (column 4, lines 24-39; column 4, lines 64-67; column 5, lines 1-8)

wherein the built-in processor and the external bus interface are responsive to respective enable signals (column 5, lines 57-67; column 6, lines 1-5; Figure 6),

and wherein one of the respective enable signals is asserted while the other one of the respective enable signals is deasserted, so that one of the built-in processor and the external bus interface corresponding to the asserted enable signal can be used exclusively (column 5, lines 57-67; column 6, lines 1-5; Figure 6).

5. As per claim 2:

The processor system according to claim 1, wherein the connection unit includes a crossbar switch (column 4, lines 64-67; column 5, lines 1-8).

6. As per claim 3:

The processor system according to claim 1, wherein the connection unit includes a common bus (column 4, lines 24-39).

7. As per claim 7:

The processor system according to claim 1, wherein the built-in processor and the external bus interface are connected through a bus common to the connection unit (column 4, lines 64-67; column 5, lines 1-8; Figure 3).

8. As per claim 8:

The processor system according to claim 1, wherein the built-in processor and the external processor use in common programs stored in memory controlled by the memory controller (column 4, lines 9-15; column 4, lines 49-50; column 2, lines 24-28) (Since the EMCPU and EXCPU use the same common memory that is controlled by the DMA controller and the EMPCU acts as the EXCPU's I/O controller when the EXCPU is present, that means that the EXCPU has to perform the actions that the EMCPU normally performs when the EXPCU is not present. Therefore they perform common programs.).

9. As per claim 9:

The processor system according to claim 1, further comprising:

an image data transfer bus connected with the connection unit (column 4, lines 2-5); and

an image output device interface or an image input device interface connected with the image data transfer bus on the semiconductor substrate (column 3, lines 66-67; column 4, lines 1-2).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Booker et al. as applied to claim 1 in view of Ozcelik et al. (US Patent 6,041,400).

12. As per claim 4:

Booker et al. do not teach a second built-in processor connected to the connection unit on the semiconductor substrate. Ozcelik et al. do (Ozcelik et al.: Figure 3, item 62).

Both Ozcelik et al. and Booker et al. teach embedded systems for controlling a television (Booker et al.: column 3, lines 27-29) (Ozcelik et al.: column 5, lines 60-63).

Ozcelik et al. comment that using multiple cores significantly reduces the complexity of the OS (Ozcelik et al.: column 3, lines 33-37).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Ozcelik's multiple cores to Booker et al. would reduce the complexity of the OS.

Response to Arguments

13. The applicant has made the following argument:

> "However, nothing in Booker is seen to disclose or suggest that a built-in processor and an external bus interface are responsive to respective enable signals, muchless that one of the respective enable signals is asserted while the other one of the respective enable signals is deasserted, so that one of the built-in processor and the external bus interface corresponding to the asserted enable signal can be used exclusively."

The examiner asserts that Booker's system is functionally equivalent to that of the application. When the EXCPU of Booker gains control of DCRX 160, it is the same as the DCRX being in control. Likewise, in the instant application, when the external bus interface 104 gains control, it is really the CPU chip 103 that is in control. The

applicant does not disclose the origin of Enable0 202, but it is assumed that it is produced by CPU chip 103. Similarly, EX_BUSREQ is asserted by EXCPU, which will hand over control from EMCPU 26 to DCRX 160.

Further, it is assumed that handshaking as described in Booker (Figure 6; column 6, line 26 to column 7, line 8) is inherent in the instant application since it is logically impossible to simply assert/deassert two signals without handshaking. The limitation described by the applicant, "wherein one of the respective enable signals is asserted while the other one of the respective enable signals is deasserted, so that one of the built-in processor and the external bus interface corresponding to the asserted enable signal can be used exclusively" is logically equivalent to Booker's handshaking system. Both BUSREQ signals will not be recognized at the same time. In the rare case where they will both be logic 1, they will not both be "asserted" simultaneously based on the handshaking mechanisms of HoldREQ and HoldACK.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ryan P Fiegle
Examiner
Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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